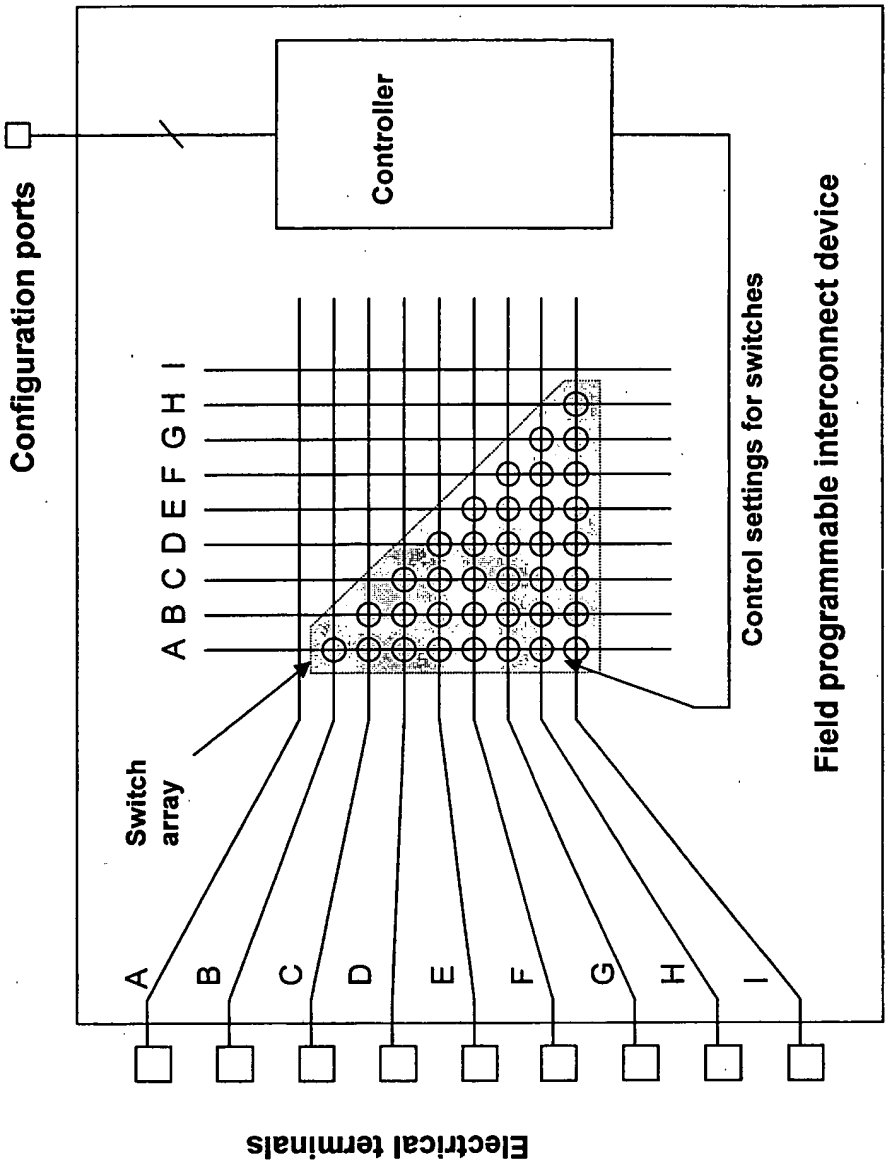


FIG. 1 (Prior Art)

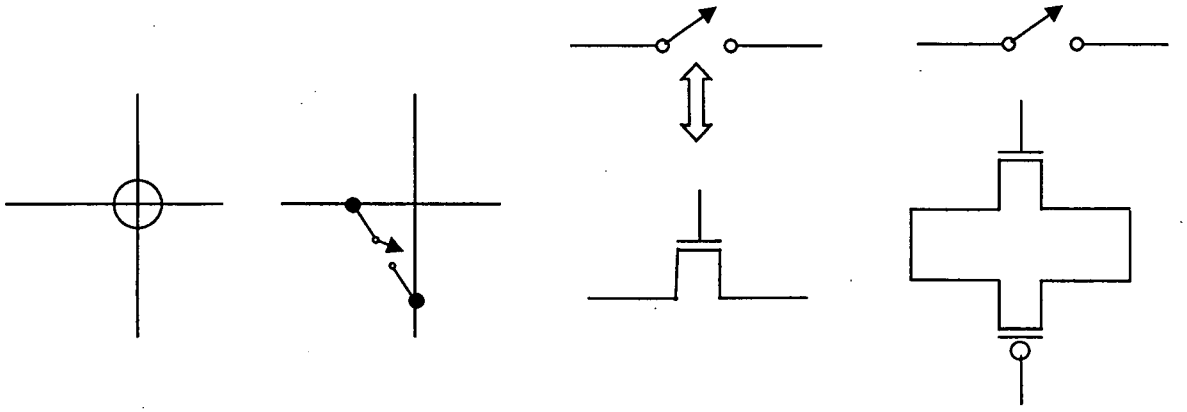


FIG. 2a FIG. 2b FIG. 2c FIG. 2d

FIG. 2 (Prior Art)

APP_ID=09683136

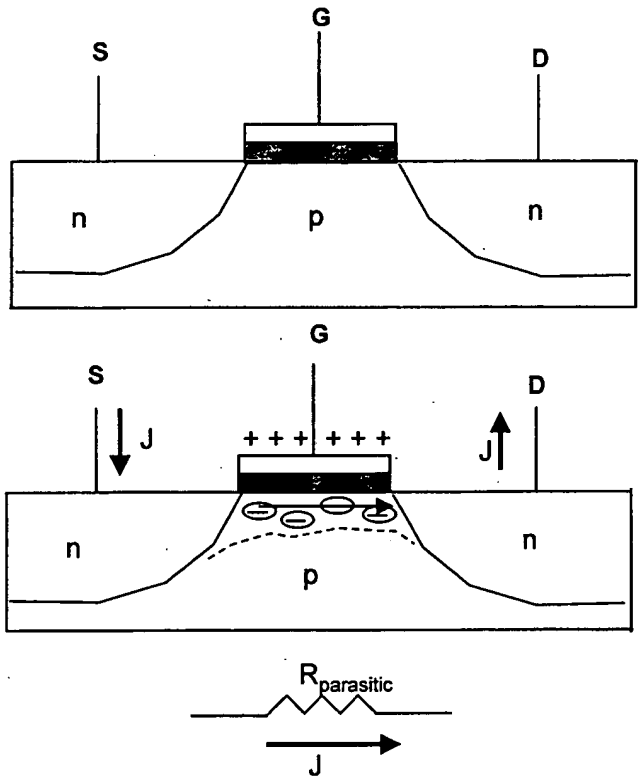


FIG. 3 (Prior Art)

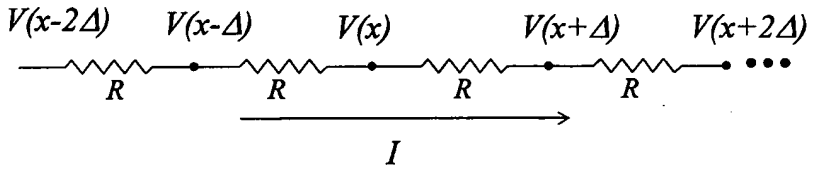


FIG. 4

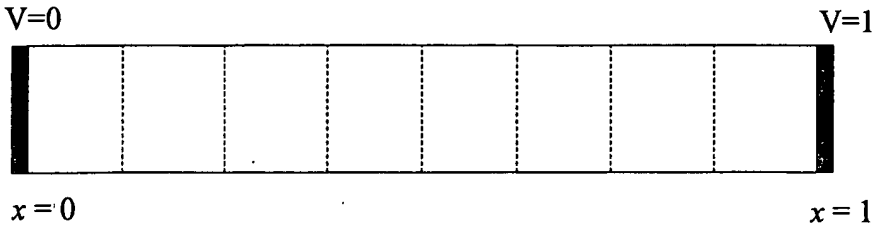


FIG. 5a

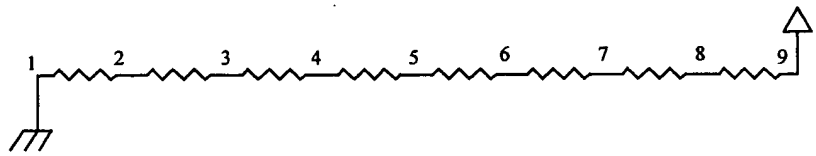


FIG. 5b

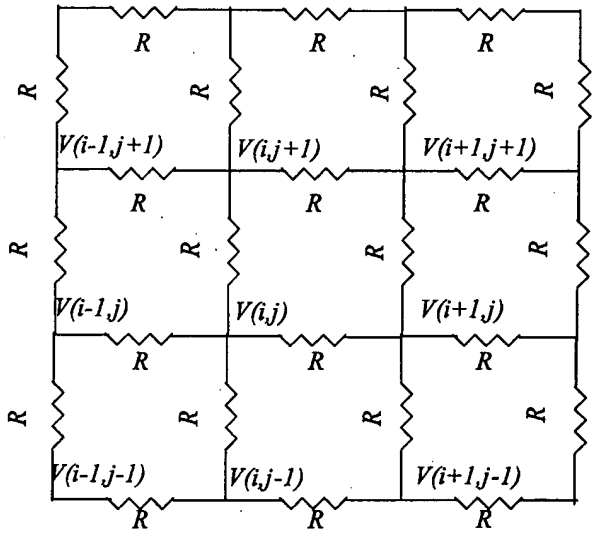

R
V(i-1,j+1)
V(i,j+1)
V(i+1,j+1)
V(i-1,j)
V(i,j)
V(i+1,j)
V(i-1,j-1)
V(i,j-1)
V(i+1,j-1)

FIG. 6a

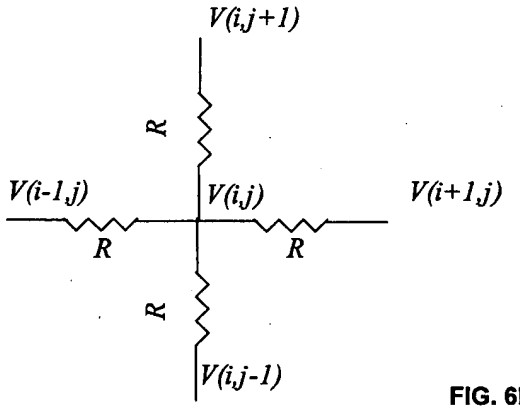
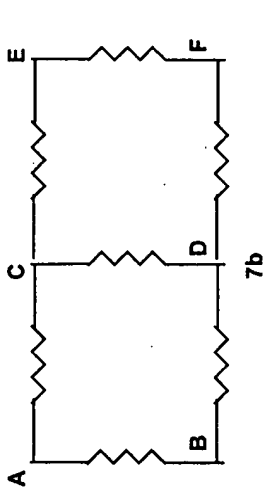
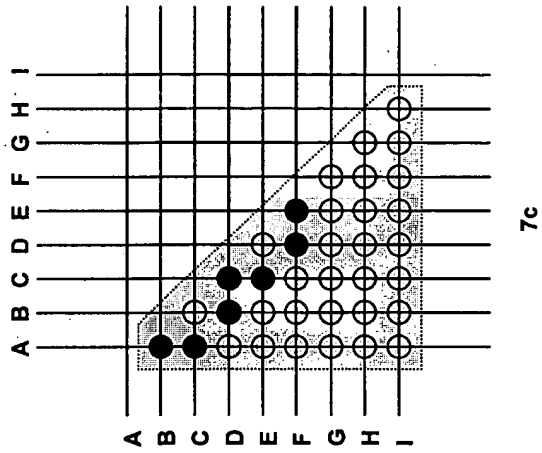

V(i,j+1)
R
V(i-1,j)
V(i,j)
V(i+1,j)
R
R
R
V(i,j-1)

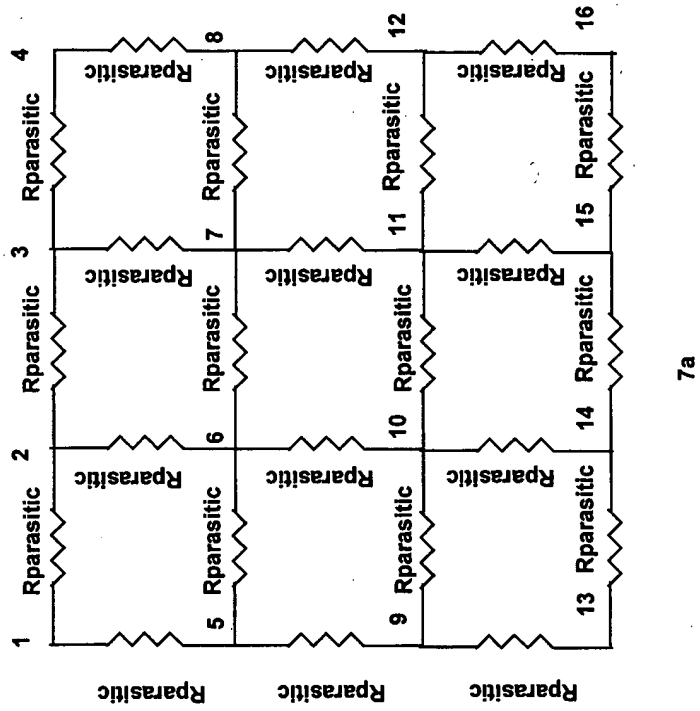
FIG. 6b


A
B
C
D
E
F

7b


A B C D E F G H I
A B C D E F G H I

7c


Rparasitic
1 Rparasitic
2 Rparasitic
3 Rparasitic
4 Rparasitic
5 Rparasitic
6 Rparasitic
7 Rparasitic
8 Rparasitic
9 Rparasitic
10 Rparasitic
11 Rparasitic
12 Rparasitic
13 Rparasitic
14 Rparasitic
15 Rparasitic
16 Rparasitic

7a

FIG. 7

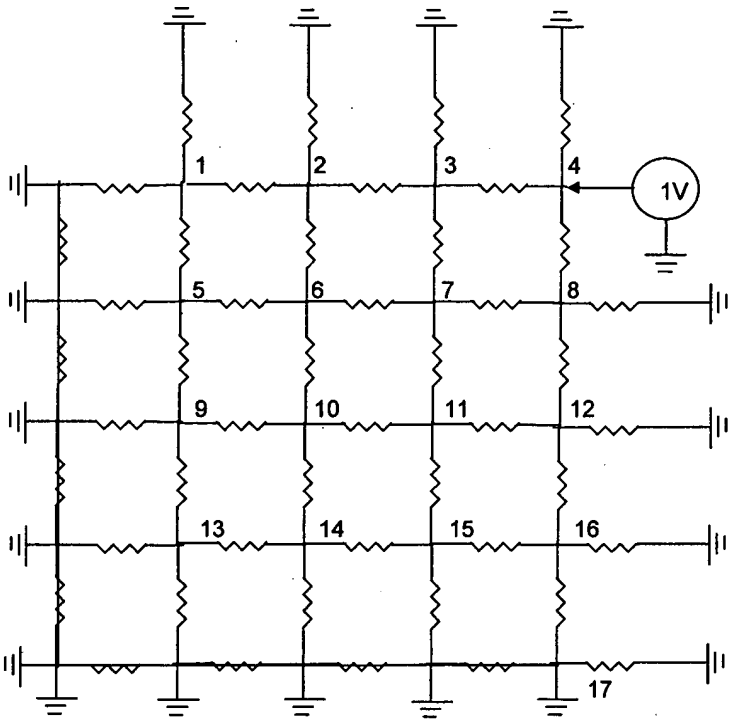


FIG. 8a

Pin	Close switches within FPID as required to connect to pin
1	2,5,17
2	6,3,17 (connection to pin 1 is already achieved)
3	4,7,17
4	8,17
5	6.9,17
6	7,10
7	8,11
8	12,17
9	10,13,17
10	11,14
11	12,15
12	16,17
13	14,17
14	15,17
15	16,17
16	17

FIG. 8b

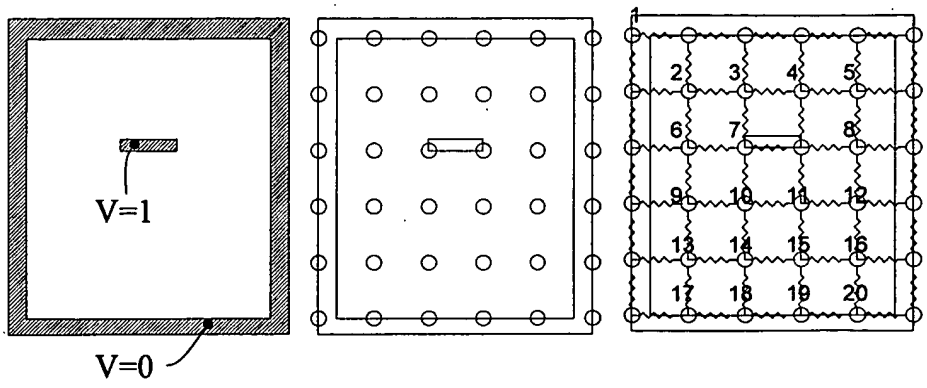


FIG. 9a

Pin #	Voltage
1	0
2	0.187919
3	0.395973
4	0.395973
5	0.187919
6	0.355705
7	1
8	0.355705
9	0.234899
10	0.47651
11	0.47651
12	0.234899
13	0.107383
14	0.194631
15	0.194631
16	0.107383

FIG. 9b

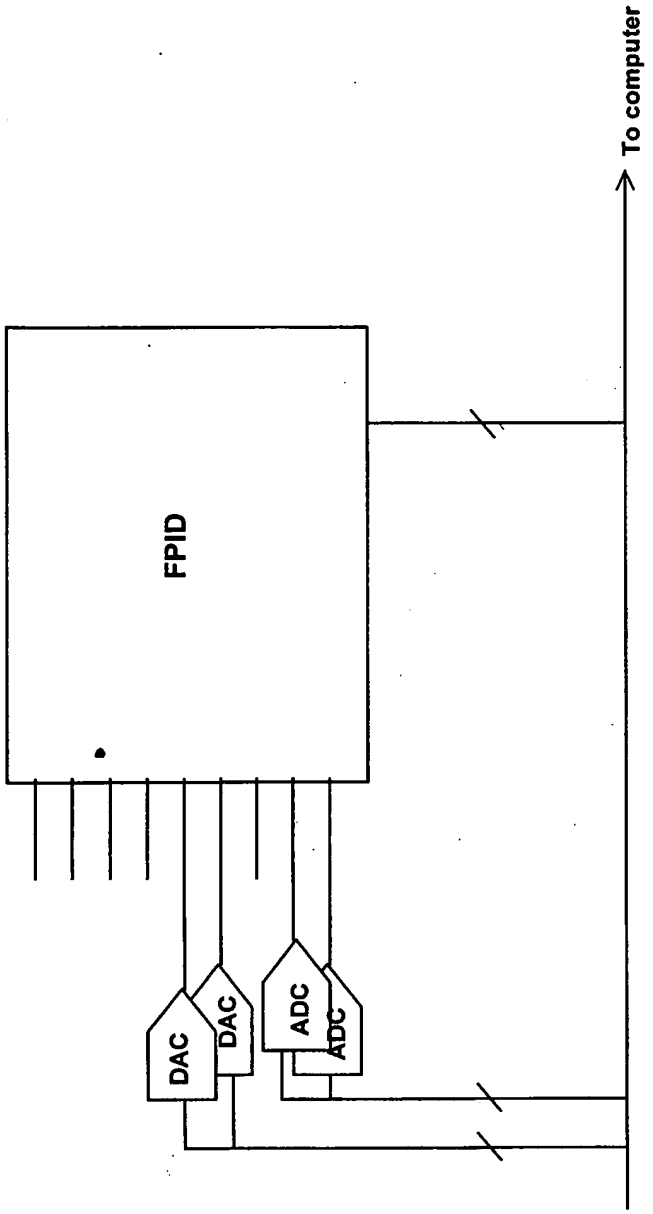


FIG. 10

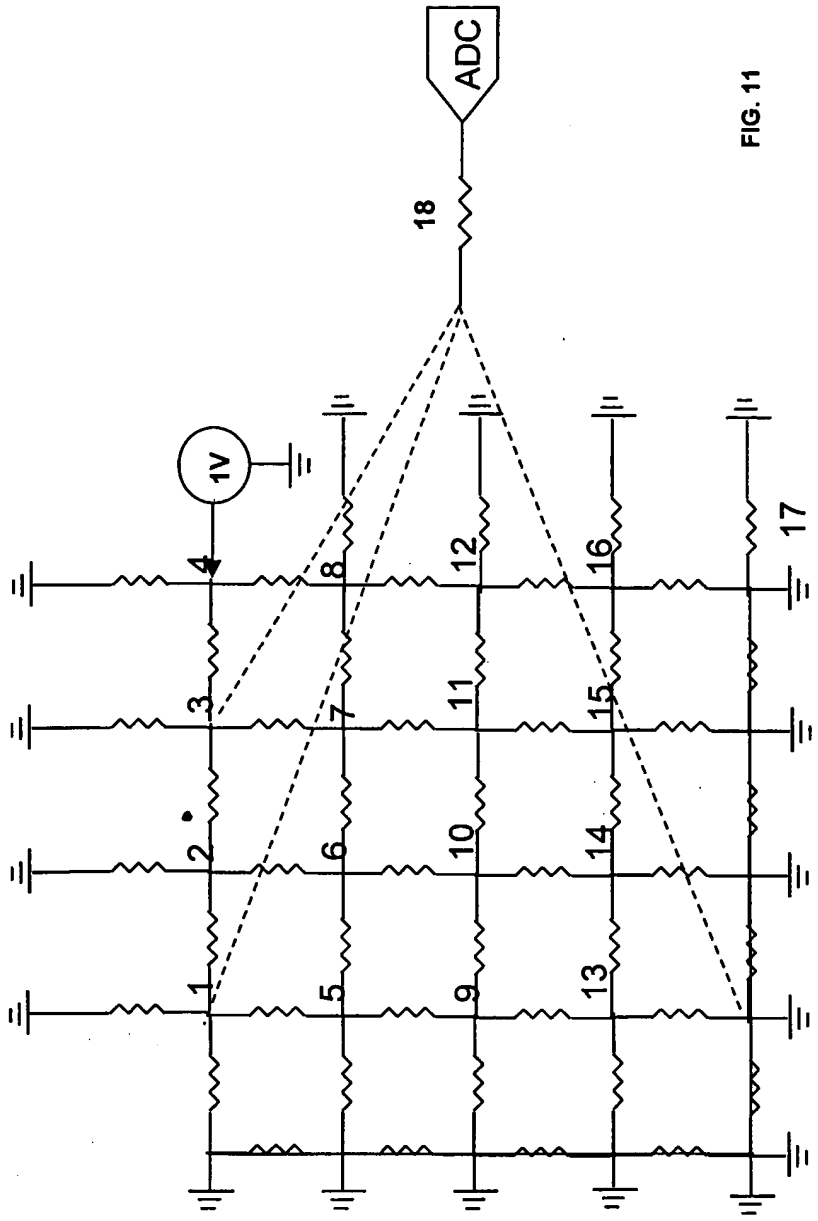


FIG. 11

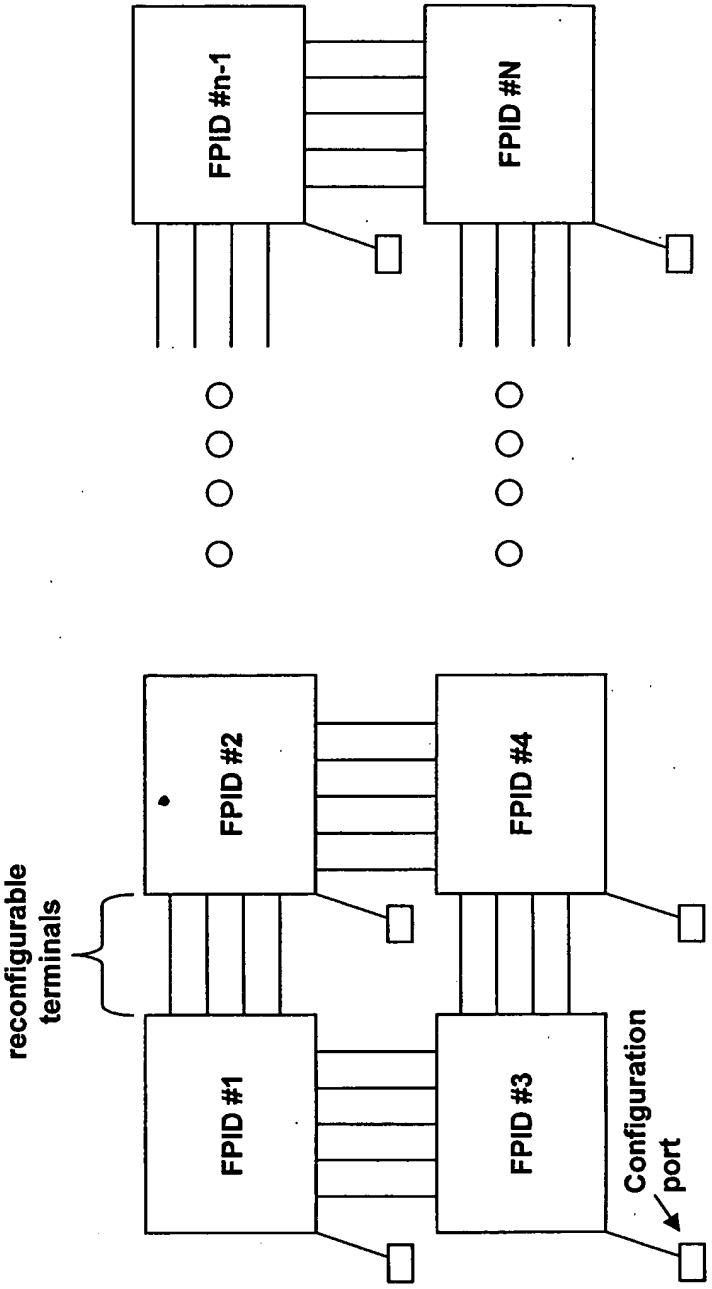
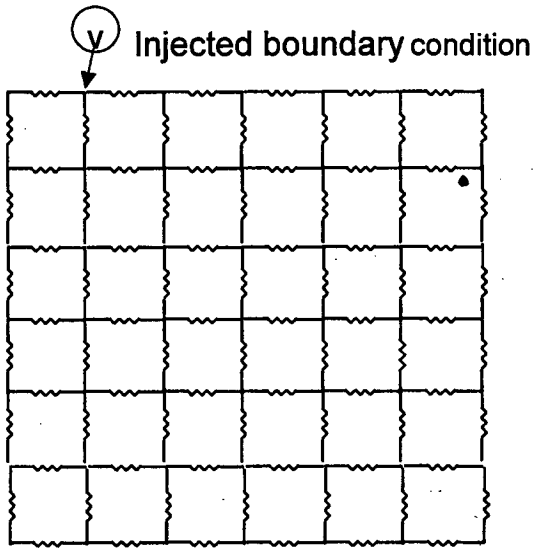
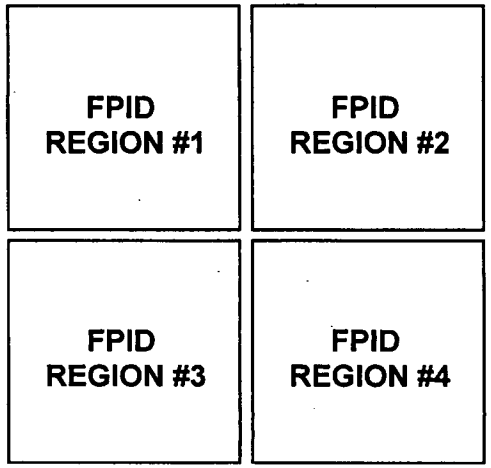

FPID #n-1
FPID #N
FPID #2
FPID #4
reconfigurable terminals
FPID #1
FPID #3
Configuration port

FIG. 12

APP_ID=09683136



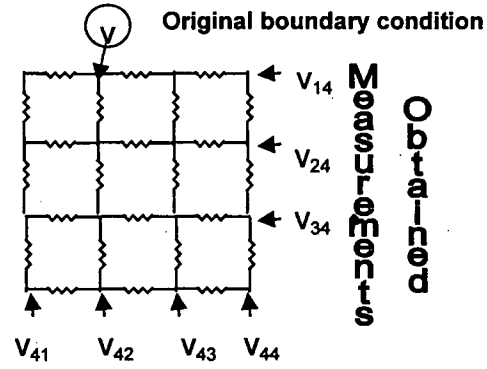
13a



13b

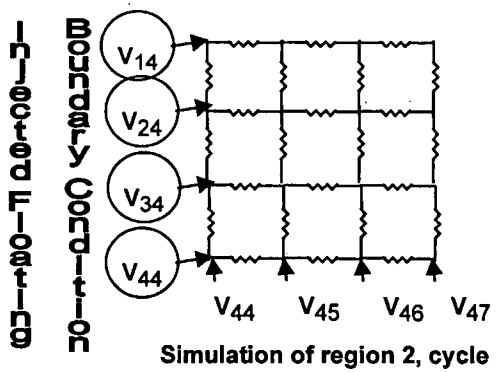
FIG. 13

APP_ID=09683136



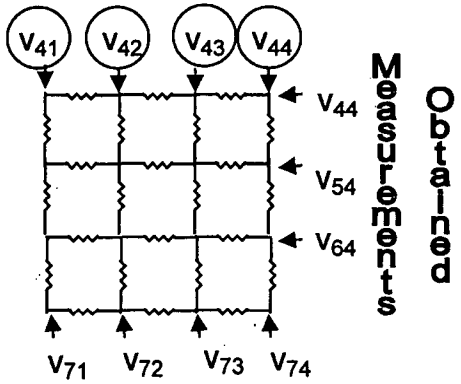
Simulation of region 1, cycle 1

14a



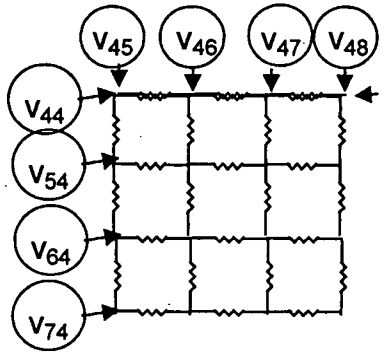
Simulation of region 2, cycle 1

14b



Simulation of region 3, cycle 1

12c



Simulation of region 4, cycle 1

14d

FIG. 14